CLAIM AMENDMENTS

141. (Currently Amended) A method of making a semiconductor package device, comprising:

attaching a semiconductor chip to a metallic structure using an insulative adhesive, wherein the chip includes a conductive pad, the metallic structure includes first and second opposing surfaces and a lead~~conductive trace~~, the adhesive is disposed between the first surface and the chip, the lead ~~conductive trace~~ includes a recessed portion, a non-recessed portion and opposing outer edges between the first and second surfaces that extend across the recessed and non-recessed portions, and the recessed portion is recessed relative to the non-recessed portion at the second surface;

forming an encapsulant that contacts the chip, the first surface, the outer edges and the recessed portion, wherein the encapsulant covers the chip, the outer edges and the recessed portion, and the non-recessed portion extends outside the encapsulant; and

forming a connection joint that electrically connects the lead ~~conductive trace~~ and the pad.

142. (Previously Presented) The method of claim 141, wherein the recessed portion is located between the non-recessed portion and the chip.

143. (Previously Presented) The method of claim 141, wherein the recessed portion is formed by etching the metallic structure.

144. (Previously Presented) The method of claim 141, wherein the recessed portion is coplanar with the non-recessed portion at the first surface.

145. (Previously Presented) The method of claim 141, wherein the recessed portion is coplanar with the non-recessed portion at the outer edges.

146. (Previously Presented) The method of claim 141, wherein the recessed portion is coplanar with the non-recessed portion at the first surface and the outer edges.

147. (Previously Presented) The method of claim 141, wherein the outer edges are defined by first and second slots in the metallic structure.

148. (Previously Presented) The method of claim 141, wherein the outer edges are formed by etching the metallic structure.

149. (Previously Presented) The method of claim 141, wherein the outer edges are formed by simultaneously etching the first and second surfaces.

150. (Previously Presented) The method of claim 141, wherein the metallic structure is a copper lead frame.

151. (Previously Presented) The method of claim 141, wherein the adhesive is the only insulator that contacts and is attached to the metallic structure before forming the encapsulant.

152. (Previously Presented) The method of claim 141, wherein the adhesive contacts the pad.

153. (Previously Presented) The method of claim 141, wherein the adhesive is spaced from a side of the chip opposite the pad.

154. (Previously Presented) The method of claim 141, wherein the adhesive is spaced from the second surface.

155. (Previously Presented) The method of claim 141, wherein the encapsulant is coplanar with the non-recessed portion at the second surface.

156. (Previously Presented) The method of claim 141, wherein the encapsulant contacts substantially none of the non-recessed portion at the second surface.

157. (Previously Presented) The method of claim 141, wherein the encapsulant contacts an entire side of the chip opposite the pad.

158. (Previously Presented) The method of claim 141, wherein the encapsulant is formed by transfer molding.

159. (Previously Presented) The method of claim 141, wherein the steps are performed in the sequence set forth.

160. (Previously Presented) The method of claim 141, wherein the device is devoid of wire bonds, TAB leads and solder joints.

161. (Currently Amended) A method of making a semiconductor package device, comprising:

providing a metallic structure that includes first and second opposing surfaces, wherein the metallic structure further includes a lead ~~conductive trace~~ and a pair of slots, the lead ~~conductive trace~~ includes a recessed portion, a non-recessed portion and opposing outer edges defined by the slots that are parallel to one another, extend between the first and second surfaces and extend across the recessed and non-recessed portions, and the recessed portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first surface, recessed relative to the non-recessed portion at the second surface and provides a channel between the slots;

attaching the metallic structure to a semiconductor chip that includes a conductive pad, wherein the first surface faces towards the chip and the second surface faces away from the chip;

forming an encapsulant that contacts the chip, the first surface, the outer edges and the recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed portion extends outside the encapsulant; and

forming a connection joint that ~~contacts and~~ electrically connects the lead ~~conductive trace~~ and the pad.

162. (Previously Presented) The method of claim 161, including forming the recessed portion and partially forming the slots by selectively etching the metallic structure from the second surface towards the first surface.

163. (Previously Presented) The method of claim 162, including partially forming the slots by selectively etching the metallic structure from the first surface towards the second surface.

164. (Previously Presented) The method of claim 161, including removing the encapsulant from portions of the slots adjacent to the non-recessed portion without removing the encapsulant from the channel.

165. (Previously Presented) The method of claim 161, wherein the encapsulant contacts an entire side of the chip opposite the pad.

166. (Previously Presented) The method of claim 161, wherein the encapsulant is coplanar with the non-recessed portion at the second surface.

167. (Previously Presented) The method of claim 161, wherein the encapsulant contacts substantially none of the non-recessed portion at the second surface.

168. (Previously Presented) The method of claim 161, wherein the encapsulant is formed by transfer molding.

169. (Previously Presented) The method of claim 161, wherein the steps are performed in the sequence set forth.

170. (Previously Presented) The method of claim 161, wherein the device is devoid of wire bonds, TAB leads and solder joints.

171. (Currently Amended) A method of making a semiconductor package device, comprising:

providing a metallic structure that includes first and second opposing surfaces;

selectively etching the metallic structure to form a pair of slots that extend between the first and second surfaces and a recessed portion that extends into the metallic structure at the second surface towards the first surface and extends between the slots, wherein the metallic structure further includes a non-recessed portion that extends between the slots, the recessed portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first surface, recessed relative to the non-recessed portion at the second surface and provides a channel between the slots, and the slots define opposing outer edges that are parallel to one another, extend between the first and second surfaces and extend across the recessed and non-recessed portions;

attaching the metallic structure to a semiconductor chip using an insulative adhesive, wherein the chip includes a conductive pad, the first surface faces towards the chip, the second surface faces away from the chip, and the recessed portion is located between the chip and the non-recessed portion;

forming an encapsulant that contacts the chip, the first surface, the outer edges and the recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed portion extends outside the encapsulant; and

forming a connection joint that ~~contacts and~~ electrically connects the metallic structure and the pad.

172. (Previously Presented) The method of claim 171, including forming the recessed portion and partially forming the slots by selectively etching the metallic structure from the second surface towards the first surface.

173. (Previously Presented) The method of claim 172, including partially forming the slots by selectively etching the metallic structure from the first surface towards the second surface.

174. (Previously Presented) The method of claim 171, including removing the encapsulant from portions of the slots adjacent to the non-recessed portion without removing the encapsulant from the channel.

175. (Previously Presented) The method of claim 171, wherein the encapsulant contacts an entire side of the chip opposite the pad.

176. (Previously Presented) The method of claim 171, wherein the encapsulant is coplanar with the non-recessed portion at the second surface.

177. (Previously Presented) The method of claim 171, wherein the encapsulant contacts substantially none of the non-recessed portion at the second surface.

178. (Previously Presented) The method of claim 171, wherein the encapsulant is formed by transfer molding.

179. (Previously Presented) The method of claim 171, wherein the steps are performed in the sequence set forth.

180. (Previously Presented) The method of claim 171, wherein the device is devoid of wire bonds, TAB leads and solder joints.

181. (Currently Amended) A method of making a semiconductor package device, comprising:

providing a metallic structure that includes first and second opposing surfaces, wherein the metallic structure further includes a lead ~~conductive trace~~ and a pair of slots, the lead ~~conductive trace~~ includes a recessed portion, a non-recessed portion and opposing outer edges defined by the slots that are parallel to one another, extend between the first and second surfaces and extend across the recessed and non-recessed portions, and the recessed portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first surface, recessed

relative to the non-recessed portion at the second surface and provides a channel between the slots;

depositing a metal trace on the metallic structure, wherein the metal trace includes a terminal that extends into the metallic structure at the first surface and a routing line that contacts the recessed portion at the first surface;

attaching the metallic structure to a semiconductor chip that includes a conductive pad, wherein the first surface faces towards the chip, the second surface faces away from the chip, the pad faces towards the first surface, the routing line extends within and outside a periphery of the chip, and the recessed and non-recessed portions are located outside the periphery of the chip;

forming an encapsulant that contacts the chip, the first surface, the outer edges and the recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed portion extends outside the encapsulant; and

forming a connection joint that contacts and electrically connects the routing line and the pad, thereby electrically connecting the lead ~~conductive trace~~ and the pad.

182. (Previously Presented) The method of claim 181, including forming the recessed portion and partially forming the slots by selectively etching the metallic structure from the second surface towards the first surface.

183. (Previously Presented) The method of claim 182, including partially forming the slots by selectively etching the metallic structure from the first surface towards the second surface.

184. (Previously Presented) The method of claim 181, including removing the encapsulant from portions of the slots adjacent to the non-recessed portion without removing the encapsulant from the channel.

185. (Previously Presented) The method of claim 181, wherein the encapsulant contacts an entire side of the chip opposite the pad.

186. (Previously Presented) The method of claim 181, wherein the encapsulant is coplanar with the non-recessed portion at the second surface.

187. (Previously Presented) The method of claim 181, wherein the encapsulant contacts substantially none of the non-recessed portion at the second surface.

188. (Previously Presented) The method of claim 181, wherein the encapsulant is formed by transfer molding.

189. (Previously Presented) The method of claim 181, wherein the steps are performed in the sequence set forth.

190. (Previously Presented) The method of claim 181, wherein the device is devoid of wire bonds, TAB leads and solder joints.

191. (Currently Amended) A method of making a semiconductor package device, comprising:

providing a metallic structure that includes first and second opposing surfaces;

selectively etching the metallic structure to form a pair of slots that extend between the first and second surfaces and a recessed portion that extends into the metallic structure at the second surface towards the first surface and extends between the slots, wherein the metallic structure further includes a non-recessed portion that extends between the slots, the recessed portion is adjacent to the non-recessed portion, coplanar with the non-recessed portion at the first surface, recessed relative to the non-recessed portion at the second surface and provides a channel between the slots, and the slots define opposing outer edges that are parallel to one another, extend between the first and second surfaces and extend across the recessed and non-recessed portions;

depositing a metal trace on the metallic structure, wherein the metal trace includes a terminal that extends into the metallic structure at the first surface and a routing line that contacts the recessed portion at the first surface;

attaching the metallic structure to a semiconductor chip using an insulative adhesive, wherein the chip includes a conductive pad, the first surface faces towards the chip, the second surface faces away from the chip, the pad faces towards the first surface, the routing line extends within and outside a periphery of the chip, the recessed and non-recessed portions are located outside the periphery of the chip and the recessed portion is located between the chip and the non-recessed portion;

forming an encapsulant that contacts the chip, the first surface, the outer edges and the recessed portion, wherein the encapsulant fills the channel and the slots, and the non-recessed portion extends outside the encapsulant; and

forming a connection joint that contacts and electrically connects the routing line and the pad, thereby electrically connecting the metallic structure and the pad.

192. (Previously Presented) The method of claim 191, including forming the recessed portion and partially forming the slots by selectively etching the metallic structure from the second surface towards the first surface.

193. (Previously Presented) The method of claim 192, including partially forming the slots by selectively etching the metallic structure from the first surface towards the second surface.

194. (Previously Presented) The method of claim 191, including removing the encapsulant from portions of the slots adjacent to the non-recessed portion without removing the encapsulant from the channel.

195. (Previously Presented) The method of claim 191, wherein the encapsulant contacts an entire side of the chip opposite the pad.

196. (Previously Presented) The method of claim 191, wherein the encapsulant is coplanar with the non-recessed portion at the second surface.

197. (Previously Presented) The method of claim 191, wherein the encapsulant contacts substantially none of the non-recessed portion at the second surface.

198. (Previously Presented) The method of claim 191, wherein the encapsulant is formed by transfer molding.

199. (Previously Presented) The method of claim 191, wherein the steps are performed in the sequence set forth.

200. (Previously Presented) The method of claim 191, wherein the device is devoid of wire bonds, TAB leads and solder joints.

201. (Previously Presented) A method of making a semiconductor package device, comprising:

providing a metal base that includes first and second opposing surfaces, wherein the metal base further includes a pair of slots that extend between the first and second surfaces, a first recessed portion that is recessed at the first surface and extends into the metal base towards the second surface and is spaced from the slots, a second recessed portion that is recessed at the second surface and extends into the metal base towards the first surface and is between and adjacent to the slots and provides a channel between the slots, and a non-recessed portion that is spaced from the first recessed portion, adjacent to the second recessed portion and between and adjacent to the slots, wherein the first recessed portion is recessed relative to the non-recessed portion at the first surface and coplanar with the non-recessed portion at the second surface, the second recessed portion is coplanar with the non-recessed portion at the first surface and recessed relative to the non-recessed portion at the second surface, and the second recessed portion and the non-recessed portion form a lead between the slots;

depositing a metal trace on the metal base, wherein the metal trace includes a terminal in the first recessed portion and a routing line on the first surface that contacts the lead;

attaching the metal base to a semiconductor chip using an insulative adhesive, wherein the chip includes a conductive pad, the first surface faces towards the chip, the second surface

faces away from the chip, the terminal is between the pad and the second recessed portion, and the second recessed portion is between the terminal and the non-recessed portion;

forming a first insulative housing portion that contacts the chip and fills the channel and the slots without contacting the terminal;

etching the metal base, thereby exposing the terminal and the adhesive;

forming a connection joint that contacts and electrically connects the routing line and the pad; and

forming a second insulative housing portion that contacts the terminal and the adhesive, wherein the terminal protrudes downwardly from and extends through the second insulative housing portion, and the first and second insulative housing portions form an insulative housing that surrounds the chip.

202. (Previously Presented) The method of claim 201, wherein forming the slots and the recessed portions includes:

forming a first etch mask on the first surface that includes openings that selectively expose the first surface;

forming a second etch mask on the second surface that includes openings that selectively expose the second surface;

applying a wet chemical etch through the openings in the first etch mask to selectively etch the first surface, thereby forming the first recessed portion and partially forming the slots;

applying a wet chemical etch through the openings in the second etch mask to selectively etch the second surface, thereby forming the second recessed portion and partially forming the slots;

removing the first etch mask; and

removing the second etch mask.

203. (Previously Presented) The method of claim 202, including:

simultaneously forming the first and second etch masks;

simultaneously applying the wet chemical etches to the first and second surfaces; and

simultaneously removing the first and second etch masks.

204. (Previously Presented) The method of claim 201, wherein depositing the metal trace includes:

forming a plating mask on the first surface that includes an opening that selectively exposes the first surface; and

electroplating the metal trace in the opening and on the exposed portion of the first surface.

205. (Previously Presented) The method of claim 201, wherein etching the metal base to expose the terminal and the adhesive includes:

depositing a protective coating on a portion of the lead that protrudes laterally from the first insulative housing portion; and then

applying a wet chemical etch that is selective of the metal base with respect to the protective coating.

206. (Previously Presented) The method of claim 205, wherein depositing the protective coating includes:

forming a plating mask on a portion of the second surface within a periphery of the first insulative housing portion that selectively exposes the portion of the lead that protrudes laterally from the first insulative housing portion; and

electroplating the protective coating on the portion of the lead that protrudes laterally from the first insulative housing portion.

207. (Previously Presented) The method of claim 201, wherein forming the second insulative housing portion includes:

depositing an insulative layer that covers the terminal; and

selectively removing a portion of the insulative layer that covers the terminal, thereby exposing the terminal without exposing a portion of the routing line that contacts the lead.

208. (Previously Presented) The method of claim 201, wherein forming the second insulative housing portion includes:

depositing an insulative layer that conformally covers the terminal; and

globally removing a surface portion of the insulative layer, thereby exposing the terminal without exposing a portion of the routing line that contacts the lead.

209. (Previously Presented) The method of claim 201, wherein the steps are performed in the sequence set forth.

210. (Previously Presented) The method of claim 201, wherein the device is devoid of wire bonds, TAB leads and solder joints.

211. (Previously Presented) A method of making a semiconductor package device, comprising:

providing a metal base that includes first and second opposing surfaces;

etching the metal base to form a pair of slots that extend between the first and second surfaces, a first recessed portion that is recessed at the first surface and extends into the metal base towards the second surface and is spaced from the slots, and a second recessed portion that is recessed at the second surface and extends into the metal base towards the first surface and is between and adjacent to the slots and provides a channel between the slots, wherein the metal base includes a non-recessed portion that is spaced from the first recessed portion, adjacent to the second recessed portion and between and adjacent to the slots, the first recessed portion is recessed relative to the non-recessed portion at the first surface and coplanar with the non-recessed portion at the second surface, the second recessed portion is coplanar with the non-recessed portion at the first surface and recessed relative to the non-recessed portion at the second surface, and the second recessed portion and the non-recessed portion form a lead between the slots;

depositing a metal trace on the metal base, wherein the metal trace includes a terminal in the first recessed portion and a routing line on the first surface that contacts the lead;

attaching the metal base to a semiconductor chip using an insulative adhesive, wherein the chip includes a conductive pad, the first surface faces towards the chip, the second surface

faces away from the chip, the terminal is between the pad and the second recessed portion, and the second recessed portion is between the terminal and the non-recessed portion;

forming a first insulative housing portion that contacts the chip and fills the channel and the slots without contacting the terminal;

removing the first insulative housing portion from a region of the slots, wherein the lead protrudes laterally from and extends through the first insulative housing portion;

etching the metal base, thereby exposing the terminal and the adhesive;

forming an opening in the adhesive, thereby exposing the pad;

forming a connection joint that contacts and electrically connects the routing line and the pad; and

forming a second insulative housing portion that contacts the terminal and the adhesive, wherein the terminal protrudes downwardly from and extends through the second insulative housing portion, and the first and second insulative housing portions form an insulative housing that surrounds the chip.

212. (Previously Presented) The method of claim 211, wherein etching the metal base to form the slots and the recessed portions includes:

forming a first etch mask on the first surface that includes openings that selectively expose the first surface;

forming a second etch mask on the second surface that includes openings that selectively expose the second surface;

applying a wet chemical etch through the openings in the first etch mask to selectively etch the first surface, thereby forming the first recessed portion and partially forming the slots;

applying a wet chemical etch through the openings in the second etch mask to selectively etch the second surface, thereby forming the second recessed portion and partially forming the slots;

removing the first etch mask; and

removing the second etch mask.

213. (Previously Presented) The method of claim 212, including:

simultaneously forming the first and second etch masks;

simultaneously applying the wet chemical etches to the first and second surfaces; and

simultaneously removing the first and second etch masks.

214. (Previously Presented) The method of claim 211, wherein depositing the metal trace includes:

forming a plating mask on the first surface that includes an opening that selectively exposes the first surface; and

electroplating the metal trace in the opening and on the exposed portion of the first surface.

215. (Previously Presented) The method of claim 211, wherein etching the metal base to expose the terminal and the adhesive includes:

depositing a protective coating on a portion of the lead that protrudes laterally from the first insulative housing portion; and then

applying a wet chemical etch that is selective of the metal base with respect to the protective coating.

216. (Previously Presented) The method of claim 215, wherein depositing the protective coating includes:

forming a plating mask on a portion of the second surface within a periphery of the first insulative housing portion that selectively exposes the portion of the lead that protrudes laterally from the first insulative housing portion; and

electroplating the protective coating on the portion of the lead that protrudes laterally from the first insulative housing portion.

217. (Previously Presented) The method of claim 211, wherein forming the second insulative housing portion includes:

depositing an insulative layer that covers the terminal; and

selectively removing a portion of the insulative layer that covers the terminal, thereby exposing the terminal without exposing a portion of the routing line that contacts the lead.

218. (Previously Presented) The method of claim 211, wherein forming the second insulative housing portion includes:

depositing an insulative layer that conformally covers the terminal; and

globally removing a surface portion of the insulative layer, thereby exposing the terminal without exposing a portion of the routing line that contacts the lead.

219. (Previously Presented) The method of claim 211, wherein the steps are performed in the sequence set forth.

220. (Previously Presented) The method of claim 211, wherein the device is devoid of wire bonds, TAB leads and solder joints.